深深圳市思科微电子有限公司
SHENZHEN SIKEWEI ELECTRONICS CO., LTD.

9435(文件编号：S&CIC0802)　30V P-Channel Enhancement-Mode MOSFET

V_{DS}= -30V

$R_{DS(ON)}$, V_{gs}@-10V, I_{ds}@-5.3A = 50mΩ@TYP

$R_{DS(ON)}$, V_{gs}@-4.5V, I_{ds}@-4.2A = 70mΩ@TYP

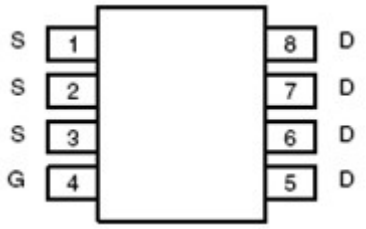
Features

Advanced trench process technology

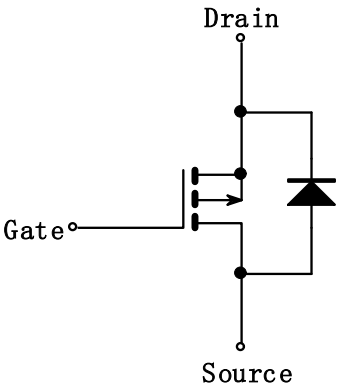
High Density Cell Design For Ultra Low On-Resistance

Improved Shoot-Through FOM

PACKAGE:　SOP-8



Internal Schematic Diagram



Maximum Ratings and Thermal Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	
Continuous Drain Current	I_D	-5.3	A
Pulsed Drain Current [1)]	I_{DM}	-20	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	℃

Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature

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Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250uA	-30	--	--	V
Drain-Source On-Stage Resistance	$R_{DS}(on)$	V_{GS} = -4.5V, I_D = -4.2A	--	70.0	90.0	mΩ
Drain-Source On-Stage Resistance	$R_{DS}(on)$	V_{GS} = -10V, I_D = -5.3A	--	50.0	60.0	
Gate Threshold Voltage	$V_{GS}(th)$	V_{DS} = V_{GS}, I_D = -250uA	-1	-1.4	-3	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V	--	--	-1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ±20V, I_{DS}=0V	--	--	±100	nA
Forward Tran conductance	g_{fs}	V_{DS} = -10V, I_D = -5.3A	--	10	--	S
Source-Drain Diode						
Max. Diode Forward Current	I_S	--	--	--	-2.6	A
Diode Forward Voltage	V_{SD}	I_S = -2.6A, V_{GS} = 0V	--	--	-1.3	V

Note: 1. Pulse test: pulse width <= 300us, duty cycle<= 2%

2. Static parameters are based on package level with recommended wire-bonding