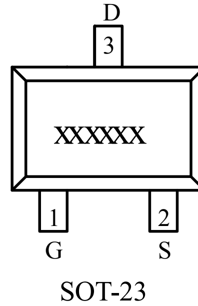
3418 (文件编号：S&CIC0937) **POWER MOSFET WAFER DATASHEET**

Feature

- 30V P-channel MOSFET High Dense Design.
- Ultra low On-Resistance.
- $R_{DS(ON)}$ <53mΩ @ V_{GS}=-10V
- $R_{DS(ON)}$ <65mΩ @ V_{GS}=-4.5V
- Reliable and Rugged
- Gross die: 38K



SOT-23

Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

Die Description

- Wafer Diameter: 8 inchs. (±0.1 inchs)
- Wafer Thickness: 8 mils. (±0.6mils)
- Die Size: 960 µm × 810µm. (Including scribe line)
- Scribe Line Width: 60µm
- Metallization: Frontside: AL/Cu, Backside: Ti/Ni/Ag.
- Metal Thickness:
  Frontside: 4µm, Backside: 1.4µm.
- Bonding Area:
  Gate: 120µm × 120µm.
  Source: Full metalized surface of source region
- Recommended Wire Bounding
  Gate: 1.5mil × 1 Au
  Source: 1.5mil × 4 Au or 2 mil × 3 Au

Electrical Characteristics (Wafer Type)

1. Absolute Maximum Ratings (TA=25℃ Unless Otherwise Noted)

Symbol.	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	±12	
I_D	Continue Drain Current	-4	A
I_{DM}	Pulsed Drain Current	-15	
I_S	Diode Continuous Forward Current	-1	A
T_J	Maximum Junction Temperature	150	℃
T_{STG}	Storage Temperature Range	-55 to 150	
$R_{\theta JA}{}^b$	Thermal Resistance-Junction to Ambient	150	℃/W

2. Static Electrical Characteristics. (TA=25℃ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	μA
		T_A=25 ℃		-30	-30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	-0.6	-0.8	-1.1	V
I_{GSS}	Gate Leakage Current	V_{DS}=±12V, V_{DS}=0V			±100	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=-10V, I_{DS}=-0.5A		43	53	mΩ
		V_{GS}=-4.5V, I_{DS}=-0.5A		50	65	
		V_{GS}=-2.5V, I_{DS}=-0.5A		60	100	
V_{SD}	Diode Forward Voltage	I_{SD}=-1A, V_{GS}=0V		-0.7	-1.3	V

Note:

a: Current maybe limit by bonding wire.

b: The $R_{\theta JA}$ is the sum of the thermal impedence from junction to ambient and depend on package type.

c: SOT23-3L package and surface mounted on 1 in^2 pad area, t ≤10 sec.

d: Pulse test; pulse width≤30μs, duty cycle≤2% (T_A=25℃ Unless Otherwise Noted)